

**TRANSMITTAL OF INFORMATION DISCLOSURE STATEMENT****(Under 37 CFR 1.97(b) or 1.97(c))**Docket No.  
**BUR920030118US1**In Re Application Of: **Gill et al.**Serial No.  
**10/708,023**Filing Date  
**02/03/2004**Examiner  
**UNASSIGNED**Group Art Unit  
**UNASSIGNED**Title: **Structure and Method for Local Resistor Element in Integrated Circuit Technology**

Address to:

**Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450****37 CFR 1.97(b)**

1. ☒ The Information Disclosure Statement submitted herewith is being filed within three months of the filing of a national application other than a continued prosecution application under 37 CFR 1.53(d); within three months of the date of entry of the national stage as set forth in 37 CFR 1.491 in an international application; before the mailing of a first Office Action on the merits, or before the mailing of a first Office Action after the filing of a request for continued examination under 37 CFR 1.114.

**37 CFR 1.97(c)**

2. ☐ The Information Disclosure Statement submitted herewith is being filed after the period specified in 37 CFR 1.97(b), provided that the Information Disclosure Statement is filed before the mailing date of a Final Action under 37 CFR 1.113, a Notice of Allowance under 37 CFR 1.311, or an Action that otherwise closes prosecution in the application, and is accompanied by one of:
- ☐ the statement specified in 37 CFR 1.97(e);
- OR**
- ☐ the fee set forth in 37 CFR 1.17(p).

**TRANSMITTAL OF INFORMATION DISCLOSURE STATEMENT**  
(Under 37 CFR 1.97(b) or 1.97(c))

Docket No.  
**BUR920030118US1**

In Re Application.

Gill et al.

MAR 10 2004

Serial No.

10/708,023

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Examiner

UNASSIGNED

Group Art Unit

UNASSIGNED

**Structure and Method for Local Resistor Element in Integrated Circuit Technology**

**Payment of Fee**

(Only complete if Applicant elects to pay the fee set forth in 37 CFR 1.17(p))

- ☐ A check in the amount of \_\_\_\_\_ is attached.
- ☒ The Director is hereby authorized to charge and credit Deposit Account No. **09-0456** as described below.
- ☐ Charge the amount of \_\_\_\_\_
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I certify that this document and fee is being deposited on **03/08/04** with the U.S. Postal Service as first class mail under 37 C.F.R. 1.8 and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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**\*This certificate may only be used if paying by deposit account.**

*Anthony J. Canale*  
Signature

Dated: **02/27/2004**

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CC:



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I hereby certify that this document is being deposited with the U.S. Postal Service, with sufficient postage, via first class mail in an envelope addressed to the Mail Stop Patent Application, Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450, on this \_\_\_\_\_ day of \_\_\_\_\_.

Signed: \_\_\_\_\_

**PATENT**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re application of:	)	Examiner:
Gill et al	)	
Serial No. <del>To be assigned</del> 10/708, 023	)	Art Unit:
Filed: Herewith 02/03/04	)	
For: <b>STRUCTURE AND METHOD FOR</b>	)	
<b>LOCAL RESISTOR ELEMENT IN</b>	)	
<b>INTEGRATED CIRCUIT</b>	)	
<b>TECHNOLOGY</b>	)	

Attorney Docket No.: BUR920030118US1 (IBU-10-5799)

**SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT**

Mail Stop Patent Application  
Commissioner for Patents  
P. O. Box 1450  
Alexandria, VA 22313-1450

Dear Sir:

This Supplemental Information Disclosure Statement is being filed to fulfill the duty of candor and good faith toward the Patent and Trademark Office, as required pursuant to 37 C.F.R. § 1.56.

Listed on the attached PTO form 1449 is information known to persons substantively involved in the preparation of the application identified above, and that a reasonable Examiner would consider important when deciding whether to allow the application. This

BUR920030118US1 (IBU-10-5799)

document is not to be construed as a representation that a search to locate the most relevant information has been made, nor a representation that more pertinent information does not exist.

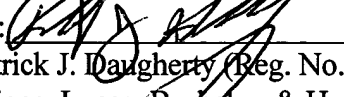
Copies of the information listed on the attached PTO Form 1449 are provided herewith.

The identification of any information herein is not intended to be, and should not be understood as being, an admission that such information, in fact, constitutes "prior art" within the meaning of applicable law. The "prior art" status of any information is a matter to be resolved during prosecution.

This Supplemental Information Disclosure Statement is being filed separately from the electronic filing of the application, which contained form PTO-1449 listing only U.S. patents and publications, and prior to an Office Action. Accordingly, it is not believed that any fee is required relating to the filing of this Supplemental Information Disclosure Statement. If this is not the case, the Patent Office is hereby authorized to charge any related fee to Deposit Account No. 09-0456.

Respectfully submitted,

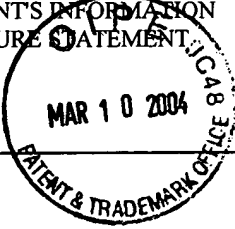
Date: December 31, 2003

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Enclosures

Subst. Form PTO-1449  
 APPLICANT'S INFORMATION  
 DISCLOSURE STATEMENT



Atty. Docket No.: BUR920030118US1 (IBU-10-5799)

Serial No.:

10/168023

Applicant: Gill et al

Filing Date: Herewith 02/03/04

Group:

### U.S. PATENT DOCUMENTS

Initial*		Document No.	Date	Name	Class	Subcl.	Filing Date
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						

### FOREIGN PATENT DOCUMENTS

		Document No.	Date	Country	Class	Subcl.	Translation?
	AJ	JP4151825A	05/25/1992	Japan	HO1L	21/28	Abstract only
	AK						
	AL						
	AM						

### OTHER DOCUMENTS

	AN	"VERTICALLY INTEGRATED LOAD RESISTOR FOR MOS STATIC RAM CELLS", IBM Technical Disclosure Bulletin, Vol. 26, No. 10B, March 1984, pgs. 5675-5677					
	AO						
	AP						
	AQ						
	AR						

Examiner:

Date Considered:

\*EXAMINER: Initial if reference considered, whether or not citation is in conformation with MPEP 609; draw line through citation if in conformance and not considered.

Include copy of this form with next communication to applicant.